

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
21 February 2002 (21.02.2002)

PCT

(10) International Publication Number
WO 02/15254 A2

(51) International Patent Classification⁷: **H01L 21/336**,
21/331, 21/8242, 21/338, 29/78, 29/739, 27/108, 29/812

Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). IN 'T
ZANDT, Michael, A., A.; Prof. Holstlaan 6, NL-5656 AA
Eindhoven (NL).

(21) International Application Number: PCT/EP01/09330

(22) International Filing Date: 9 August 2001 (09.08.2001)

(74) Agent: **STEVENS, Brian, T.**; Internationaal Octrooi-
reau B.V., Prof Holstlaan 6, NL-5656 AA Eindhoven (NL).

(25) Filing Language: English

(81) Designated States (*national*): JP, KR.

(26) Publication Language: English

(84) Designated States (*regional*): European patent (AT, BE,
CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC,
NL, PT, SE, TR).

(30) Priority Data:
0020126.9 17 August 2000 (17.08.2000) GB
0101690.6 23 January 2001 (23.01.2001) GB

Published:

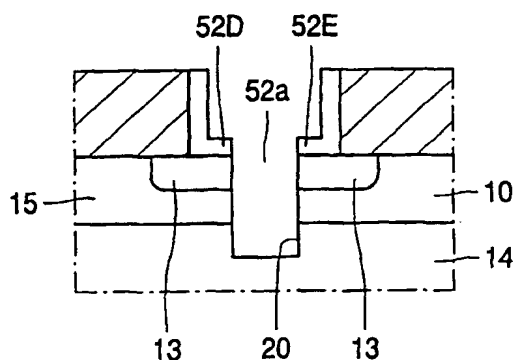
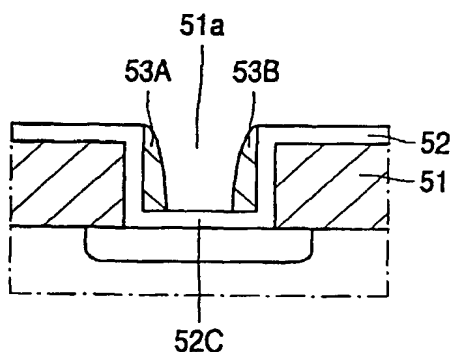
— without international search report and to be republished
upon receipt of that report

(71) Applicant: **KONINKLIJKE PHILIPS ELECTRON-
ICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA
Eindhoven (NL).

For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(72) Inventors: **HUETING, Raymond, J., E.**; Prof. Holstlaan
6, NL-5656 AA Eindhoven (NL). **HIJZEN, Erwin, A.**;

(54) Title: MANUFACTURE OF TRENCH-GATE SEMICONDUCTOR DEVICES



(57) Abstract: The manufacture of a trench-gate semiconductor device, for example a power transistor or a memory device includes the steps of forming at a surface (10a) of a semiconductor body (10) a first mask (51) having a first window (51a), providing a thin layer of a second material (52) in the first window (51a), forming an intermediate mask (53A, 53B) of a third material having curved sidewalls and using the intermediate mask (53A, 53B) to form two L-shaped parts (52A, 52D and 52B, 52E) of the second material with a second window (52a) which is used to etch a trench-gate trench (20). The rectangular base portion (52D, 52E) of each L-shaped part ensures that the trench (20) is maintained narrow during etching. Narrow trenches are advantageous for low specific on-resistance and low RC delay in low voltage cellular trench-gate power transistors. Narrow deep trenches are also advantageous for cell density in DRAM devices where a memory cell has a switching transistor cell surrounded by a trench-gate and a storage capacitor in a lower part of the same trench.

WO 02/15254 A2